48.

FREQUENCY MODULATION / DEMODULATION

606

Introduction :- This board is designed to study of frequency modulation by VCO type modulator. The synchronized modulation signal is generated within the board and demodulation is carried out by PLL. IC regulated power supply is incorporated for operation.

Brief theory :- In frequency modulation the frequency of carrier wave is altered in such way by a low frequency modulating wave to transmit the information from one site to other through air. The advantage of frequency modulation is that there is no change in its amplitude from outer world interfearences and particularly a wider bandwidth which makes very faithful receptions of music signals, generally called the high fidelity transmission. The frequency modulation is defined by a useful parameter called the '*frequency deviation*' which determine the bandwidth of the signal. In laboratory practicals narrowband FM is generated by reactance modulators or by voltage controlled oscillators. This narrowband frequency modulated signal when goes through frequency multipliers it form wideband FM signal.

The power contents in FM signal derived by 'Parseval' theorem which states that the total power of the signal is equal to the sums of the power of individual componenets presented in it. As FM signal has same amplitude in modulated or unmodulated form thus it is find out that the power is same in both cases.

Bandwidth of FM signals depends upon the modulation index which is equal to total deviation in frequency / frequency of modulating signal

$$mf = \Delta f / fm$$

From the modulation index Bessel function can be determined which helps to plot the frequency modulation spectrum. The modulator effieciency is calculated as

$$\text{Modulator efficiency } kf = \Delta f / V fm \qquad \text{Hz / volt}$$

where V fm is the peak amplitude of the input modulating signal.

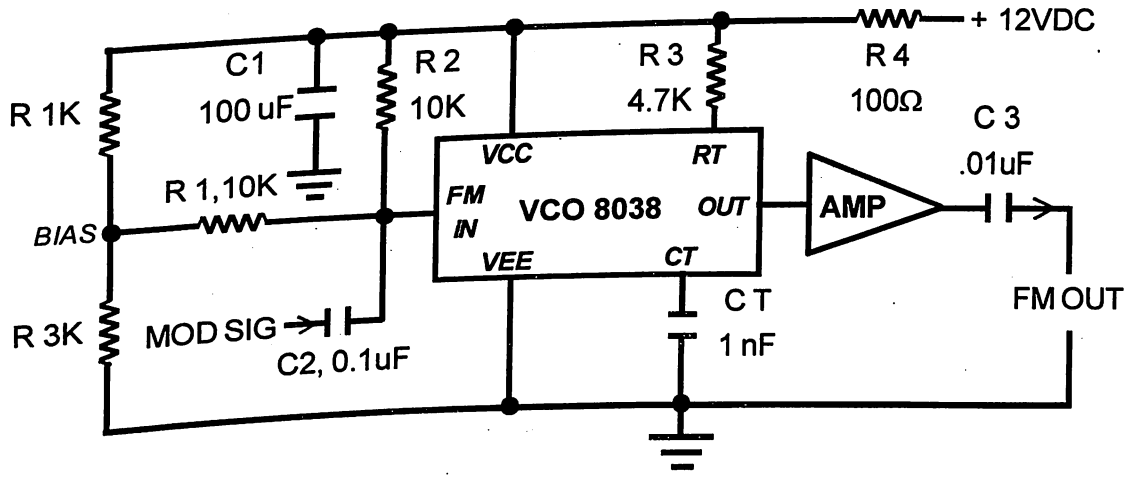


Fig 1 : Voltage controlled oscillator ICL 8038 as FM modulator.

The modulator circuit :- In fig 1, given VCO chip ICL 8038 circuit shown where it perform the function of frequency modulator. The 8038, is basically used for waveform generation. The generated frequency is determined primarily by the timing resistor **RT** (R3) , the timing capacitor **CT** and the (dc) bias voltage at FM input. In present circuit resistor R2 in conjuction with R1 and voltage divider (R1K & R3K) determine the free run frequency, which may be consider as **carrier frequency**. External modulating signal can be inserted at appropriate input through dc blocking capcitor C2. The free run frequency (carrier) of the VCO changes in rythem of input signal polarity and amplitude hence frequency modulation achieved. The obtained signal is furthur amplified by an amplifier and terminated to FM out sockets through dc blocking capacitor C3.

The signal source :- As stated earlier that VCO itself generate the free run frequency called carrier. Addition to that the board has built in 2 Khz (approx) phase synchronized AF generator MOD SIG with amplitude 0 - 3 Vpp approx. The output impedance of the modulator is 1K ohms.

A synchronization signal is given to trigger CRO in external trigger mode.

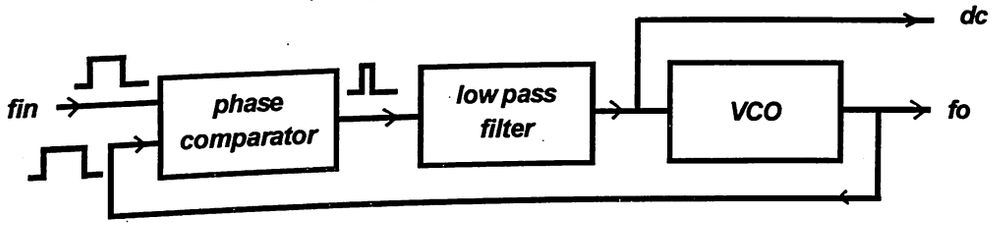


Fig 2 : Phase lock loop system

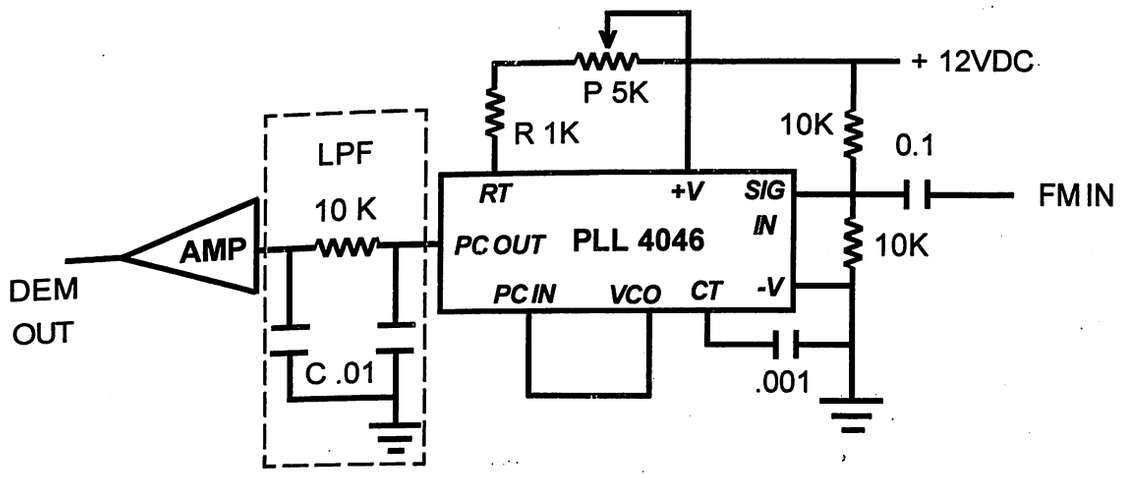


Fig 3 : Phase lock loop IC NE 565 as FM demodulator.

The PLL :- The phase lock loop (PLL) consists of a free run voltage controlled oscillator (VCO)and a digital phase comparator circuit. The prime aim of it to generate a signal of such frequency (fo) which has same frequency (fin) as at the phase comparator input. Let see the fig 2, where basic block diagram of such PLL is shown. The VCO free run signal is connected back to one input of phase comparator. The phase comparator give an output pulse, the width of which is the difference between two signal phase one from outside (fin) and other from VCO (fo). The output signal is passed through low pass fiter to form dc voltage which is used to control free run frequency of VCO. This process of 'tracking' is continued (called capture process) till both fin and fo 'held' same phase/ frequency (called lock). The phenomenon 'track and hold' of phase lock loop is used to demodulate the frequency modulated signal.

In fig 3, the circuit of frequency demodulator using IC CD4046 is shown. The IC has inbuilt

voltage controlled oscillator (the free run frequency of which depends upon control voltage from PC out, the timing resistor RT and timing capacitor CT), a phase comparator an amplifier and inbuilt 3.6K Ohm resistor connected between VCO sig in and PC out. In present circuit RT is made variable using potentiometer 5K (P) to bring VCO free run frequency close to carrier frequency for proper tracking. The PC out is filtered by two ,01 uF capacitors and furthur amplified to recover the modulating signal.

The frequency demodulation by PLL : When unmodulated carrier is feed to PLL signal input and RT (**P**) assummed to adjusted for same free run frequency as input the PC out has no pulse since fin = fo, the output at PC is assummed zero. When modulated signal is feed at input the PC output has different width of pulses, since the input signal is contineously deviating. The deviating dc voltage at PC out is used to track VCO and same is amplified by passing through LPF to recover the modulating signal. The capture range of 4046 has 1:4 ratio of its free run frequncy thus at 64Khz carrier it demodulate ±15Khz deviated signal only.

Experiment procedure : Study of FM modulation by VCO.

Other apparatus required : A dual trace CRO

1. Connect the modulating signal socket (MOD SIG in box) with the MOD SIG socket in modulator circuit. Keep amplitude control at minimum. Givenmod sig frequency is 2Khz.

2. Connect CRO with the FM OUT socket and ground. Display the signal upon CRO and measure its unmodulated frequency (1/T) with calibrated time base of CRO (about ..... Khz).

3. Now connect CRO other channel with the MOD SIG socket. Adjust amplitude control of modulating signal to 2.5 Vpp. Trigger CRO* with this signal. Note its amplitude as Ain.

4. Observe the modulated signal. Trace it upon paper. Measure the maximum frequency deviation by using X magnification (easy to measure at -ve slope of modulating signal).

5. Now from the observations

a) Unmodulated carrier frequency ..... Khz

b) Modulated and deviated carrier frequency ..... Khz (at -ve slope of mod sig)

The frequency deviation is Δf = (a) - (b) ..... Khz

Total deviation at both slopes of mod signal is $2\Delta f$ in ..... $\pm$ Khz

The modulating signal fm ..... Khz

The mod index (modulation factor) mf = $2\Delta f / fm$

The mod signal amplitude Ain..... Vpp

The modulator efficiency Kf = $2\Delta f$ / Ain Khz/Vpp

6. Compute the result from observations.

From observation it is found that mf is changed with fm, but Δf is not changed. the Δf is a function of fm amplitude.

Demodulation : To obtain frequency demodulated signal by PLL demodulator.

1. Remain the CRO one channel A, with the **MOD SIG** socket as earlier. disconnect the 2nd channel B, from **FM out** and connect it with the PLL **VCO** out TP. Keep the mod signal amplitude minimum. The given fm is = 2Khz.

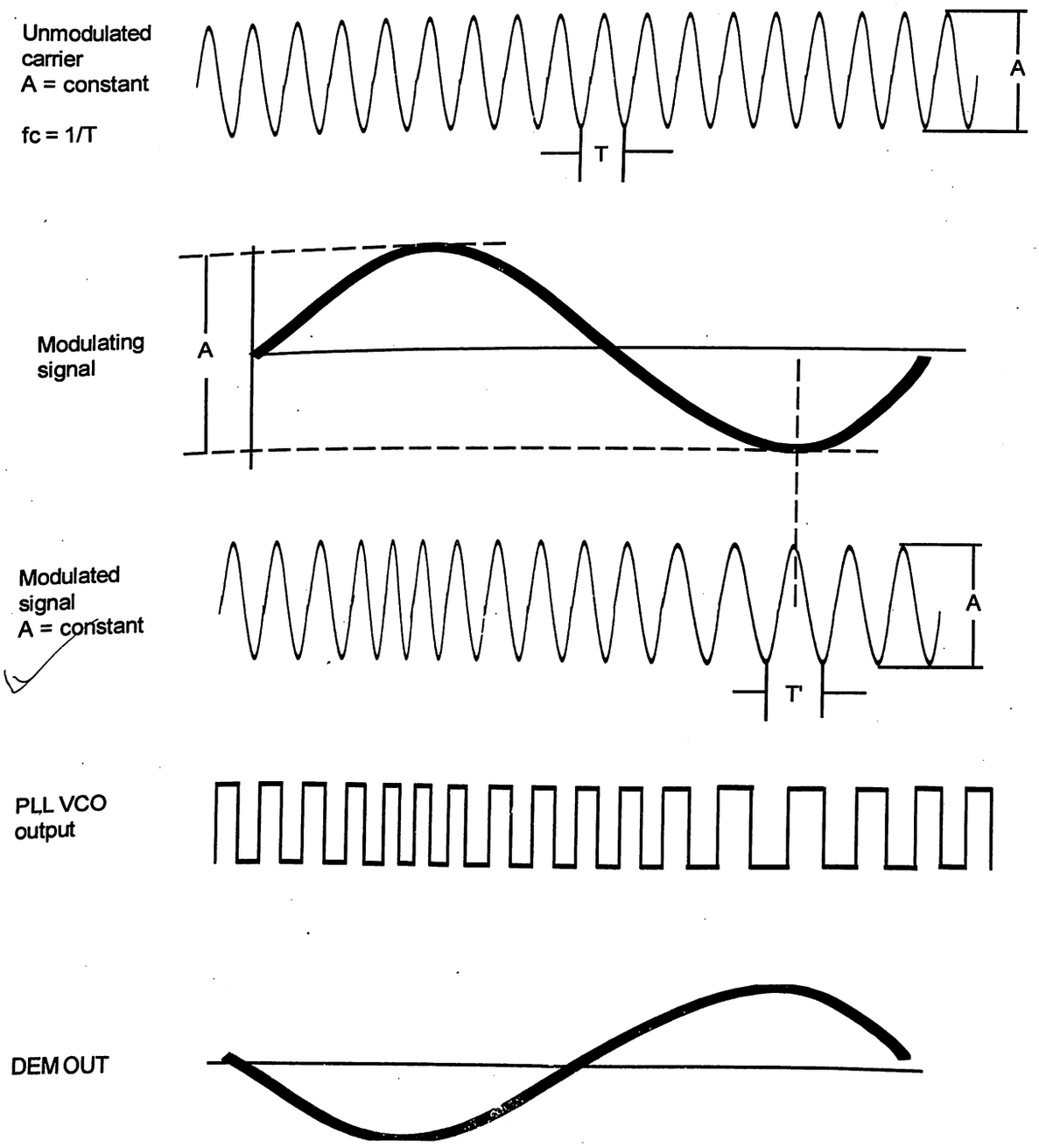
2. Connect **FM out** with PLL demodulator **FM IN** socket.

3. Trigger CRO with the 2nd channel B, to observe VCO signals. Move the pot **FREE RUN** and observe its effect upon the VCOsignal.

4. Connect CRO 2nd ch with DEM OUT.

5. Move **FREE RUN** to obtain maximum output. Trigger CRO with channel A. There is phase difference due to LPF and amplifier.

For CRO external trigger mode : To observe the modulating and modulated signal trigger CRO with modulating signal otherwise trigger it with SYNC signal connecting it with ext trigger input of CRO.



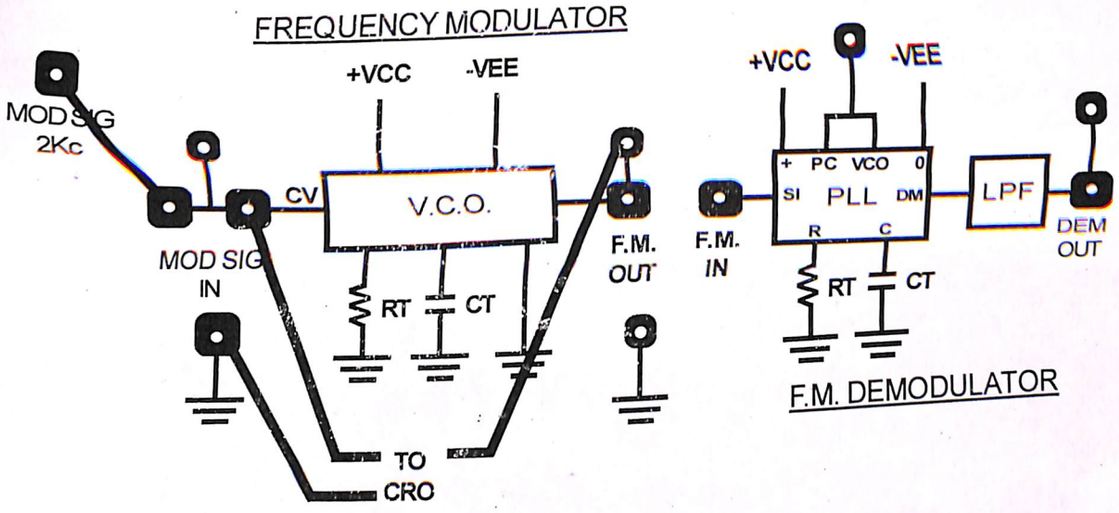


Fig 4 : Connections for Freq modulation.

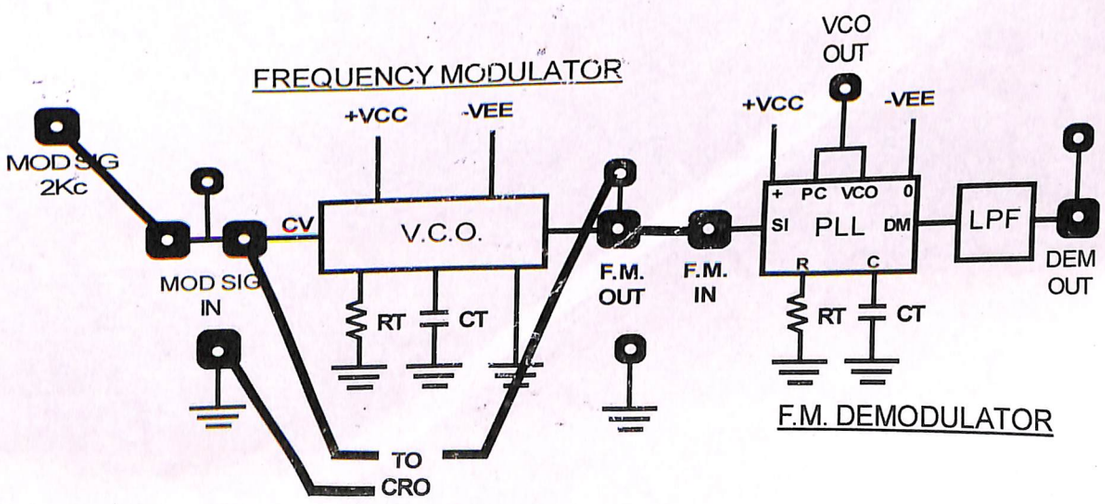


Fig 4 : Connections for Freq demodulation.

Half substractor

In substraction the relative magnitudes of input bits is checked as 1 and 0. Assume the input bits are A(minuend) and B (subtrahend). Four possibilities are shown in table below.

Table of half substractor

	Input bits		output	
	A	B	Borrow	Difference
1	0	0	0	0
2	0	1	1	1
3	1	0	0	1
4	1	1	0	0

In case one & four, both inputs are even, there is no change in output since zero minus zero is zero and one minus one is also zero. In case two the minuend bit is zero and subtrahend is one. So one is borrowed from next significant bit and output indicate the result as - 1. The minus (-) indicate the borrowed bit from next stage which has value of 2. Thus the result is 2 - 1 = 1 or 0 - 1 = - 1, with 1 borrowed. The third case is also simple one - zero = one. A logic circuit is made to perform these function is shown below. The NOT gate is included in half adder circuit which makes AND, true if minuend is smaller than subtrahend.

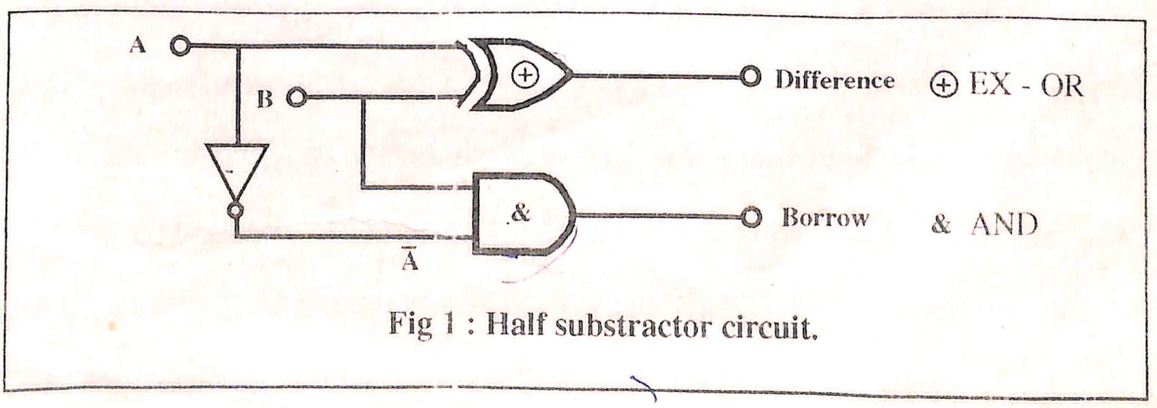


Fig 1 : Half substractor circuit.